by linking its counting input to an overflow output of the elementary counter of the lower stage to constitute a global addressing counter, the process comprising:

using, for addressing of the stage of switches of lower level closest to the inputs of the multiplexer, an elementary counter having a capacity or counting cycle length that can be adjusted on command;

providing controllable circuits for shunting the elementary counters of the stages of intermediate switches;

periodically generating a counting order for the counting input of the elementary counter of the stage of switches of lower level to describe successive counting cycles;

altering a configuration of the global addressing counter, at a start of each of the counting cycles of the elementary counter of the stage of switches of lower level, by acting on a length of a forthcoming counting cycle of this elementary counter of the stage of switches of lower level as well as on in-activity shunting circuits of the elementary counters of the stages of intermediate switches.

14. (New) Process according to claim 13, wherein successive reconfigurings of the global counter for addressing the multiplexer occur in a scanning sequence for the inputs of the multiplexer, and are defined with aid of a string of instructions written in a binary reconfiguring language comprising code words for adjusting a length of the counting cycle of the elementary counter catering for addressing of the stage of switches of lower level and code words for activating or inhibiting the controllable shunting circuits of the elementary counters catering for addressing of the stages of intermediate switches.

15. (New) Process according to claim 14, wherein the language for reconfiguring the global counter for addressing the multiplexer also comprises code words for activating or inhibiting a mode for repeating or for retaining the length of the counting cycle of the

elementary counter catering for the addressing of the stage of switches of lower level and a repetition code word valid only when the repetition mode is active.

16. (New) Process according to claim 14, wherein the language for reconfiguring the global counter for addressing the multiplexer comprises an end code word indicating an end of a string of configuration instructions.

17. (New) Process according to claim 14, wherein the code words of the language for reconfiguring the global counter for addressing the multiplexer are binary code words of variable lengths, the code words most frequently used having shortest lengths.

18. (New) Process according to claim 15, wherein various binary code words of the language for reconfiguring the global counter for addressing the multiplexer all begin with a 0 with exception of a code word for inhibiting a repetition mode.

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19. (New) Process according to claim 15, wherein the repetition code word in the language for reconfiguring the global counter for addressing the multiplexer is logical 0.

20. (New) Process according to claim 15, wherein the code word for inhibiting the repetition mode in the language for reconfiguring the global counter for addressing the multiplexer is logical 1.

21. (New) Process according to claim 15, wherein the code word for activating the repetition mode in the language for reconfiguring the global counter for addressing the multiplexer is binary 01.

22. (New) Process according to claim 15, applied to a multiplexer with three stages of switches, wherein the code words for activating and for inhibiting the controllable circuit for shunting the elementary counter addressing the second stage of switches in the language for reconfiguring the global counter for addressing the multiplexer coincide and are expressed by the binary word with four bits 0001, this binary word signifying a change of an

active or inactive state of the shunting circuit of the elementary counter addressing the second stage of switches.

23. (New) Process according to claim 16, wherein an end code word in the language for reconfiguring the global counter for addressing the multiplexer is a string of binary zeroes.

a1 24. (New) Addressing device for a multiplexer having a staged architecture with plural stages of switches from its input to its output, comprising a global counter including a chaining of elementary counters each addressing a stage of switches of the multiplexer, comprising a global counter with an elementary counter having counting capacity configured to be adjusted on command for the addressing of the stage of switches of lower level closest to the inputs of the multiplexer and with controllable circuits for shunting its elementary counters addressing the stages of intermediate switches, and a handler running a sequence of commands for reconfiguring the counter in accomplishment of its counting cycle.

IN THE ABSTRACT

Please cancel the original Abstract on page 31 in its entirety and insert therefor:

ABSTRACT

The systematic, and possibly repeated, acquisition of several distinct quantities with a view to their exploitation by a user system. The acquisition is effected by a multiplexer with staged architecture not having all of its inputs hard-wired. In such a case, the multiplexer is a2 addressed at the level of each of its stages by an elementary counter chained with elementary counters catering for the addressing of lower stages. The scanning of the inputs is achieved by regularly incrementing the chain of counters. If no precaution is taken, all the inputs of the multiplexer are scanned without taking account of their possible absences. To remedy